

AMENDMENTS TO THE DRAWINGS

The proposed drawing correction filed on March 21, 2003 has been disapproved because it is not in the form of a pen-and-ink sketch showing changes in red ink or with the changes otherwise highlighted. See MPEP 608.02(v). The objection to the drawings in the previous office action of February 20, 2003, paragraphs 6 and 7 is not withdrawn.

Applicant apologizes for the inconvenience and was following the proposed revised amendments under 37 C.F.R. §1.121 that were in place at the time the proposed drawing corrections were filed and indicated that "Amendments to the drawing figures shall be made by presenting replacement figures which include the desired changes, without markings, and which comply with § 1.84. The changes shall be explained in the accompanying remarks section of the amendment paper."

The Examiner has objected to Figures 23, 27, 28, 41-46, 61, 62, 68 and 69 as failing to comply with 37 CFR §1.74 because they do not include reference signs. In response, Applicant is representing replacement Figures 23, 27, 28, 41-46, 61, 62, 68 and 69 that incorporate proposed changes including number elements tying them to the written specification. In addition, Applicant is including annotated sheets showing changes to Figures 23, 27, 28, 41-46, 61, 62, 68 and 69. As a result, Applicant is requesting withdrawal of this objection.

Attachment: Replacement Sheets 23, 27, 28, 41-46, 61, 62, 68 and 69.

Annotated Sheets Showing Changes 23, 27, 28, 41-46, 61, 62, 68 and 69.

Additional Sheet for New Figure 124.

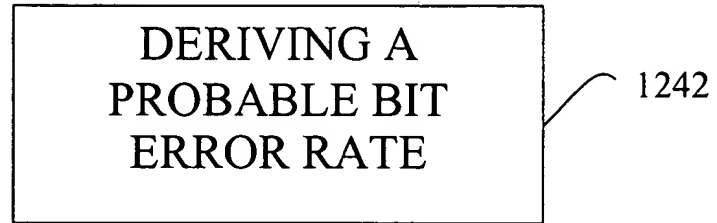


FIG. 124

600-850MHz
INPUT
(LIMITED TO
100MHz)

152
100MHz
BPF

154
VOLTAGE
TUNED
FILTER

156
VOLTAGE
TUNED
FILTER

158
VOLTAGE
TUNED
FILTER

160
A/D

162
A/D

164
SAMPLE
BUFFER

176
DESCRAMBLER

178
SERIAL
PORTS

PAYLOAD
(8 DS0+s)

IOC

156
DAC

158
DAC

173
CLOCK
GENERATOR
(EPLD)

2 KHz SUPERFRAME
8 KHz FRAME CLK
SAMPLE CLOCK
FRAME CLOCK (16 KHz)
PAYLOAD DATA TIMING(TBR)
IOC TIMING

172
CARRIER
AMPLITUDE
TIMING
RECOVERY

166
DOWN
CONVERTER
COMPENSATION

180
FFT
32 POINT

174
EQUALIZER
(VECTOR
ROTATION)

174
SYMBOLS
TO
BITS

SIGNAL PROCESSOR LOADED ABOUT 50%

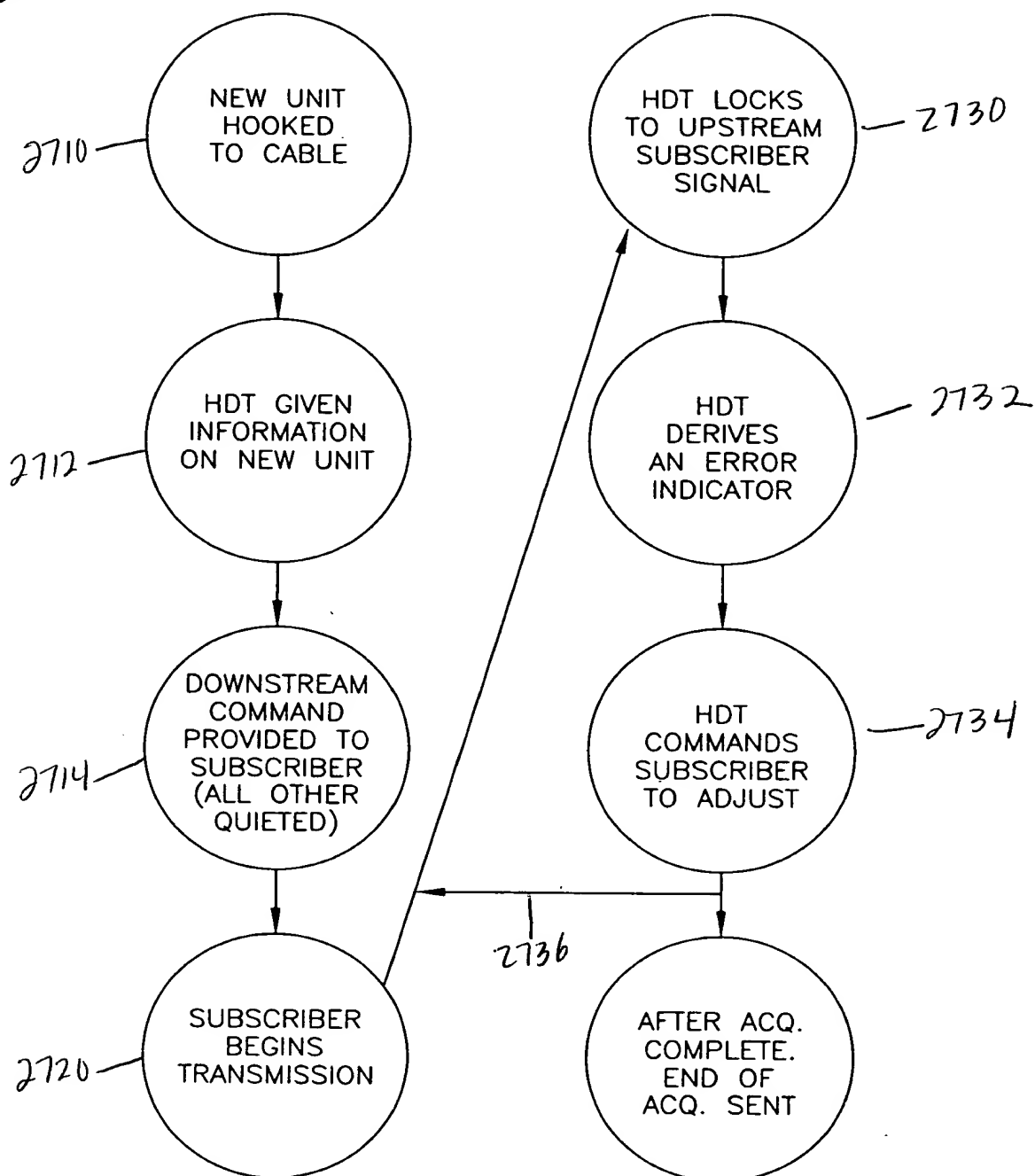


FIG. 27





Annotated Sheet Showing Changes

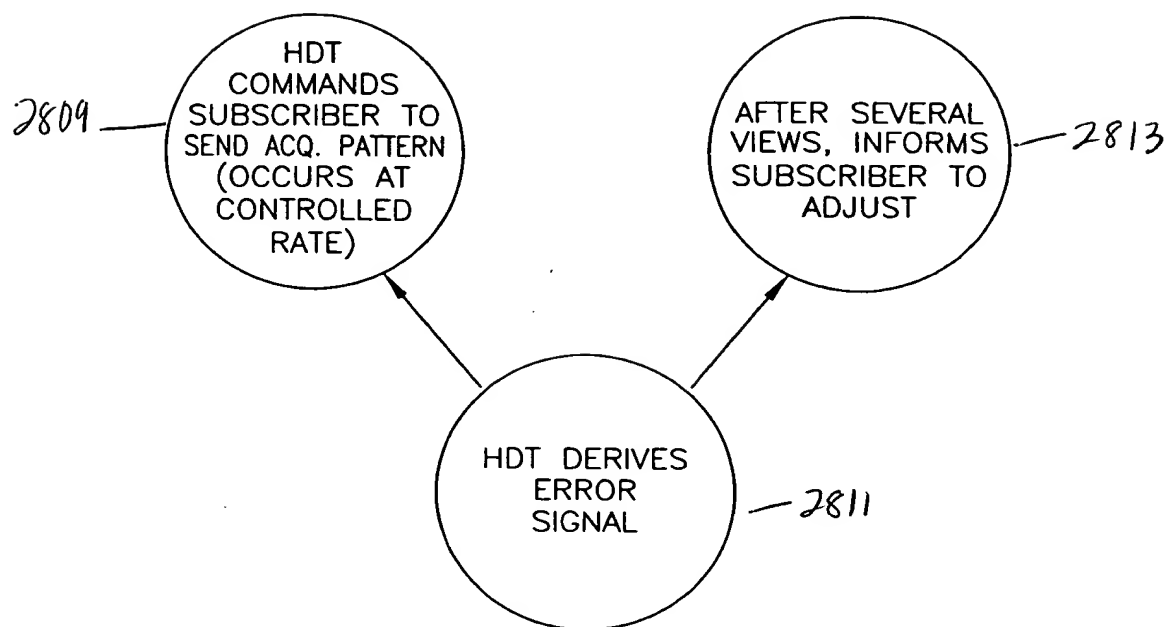


FIG. 28

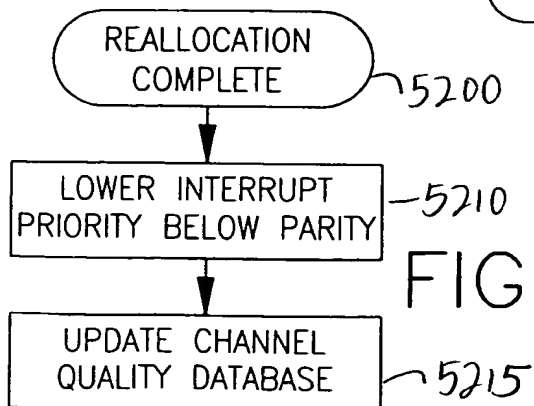
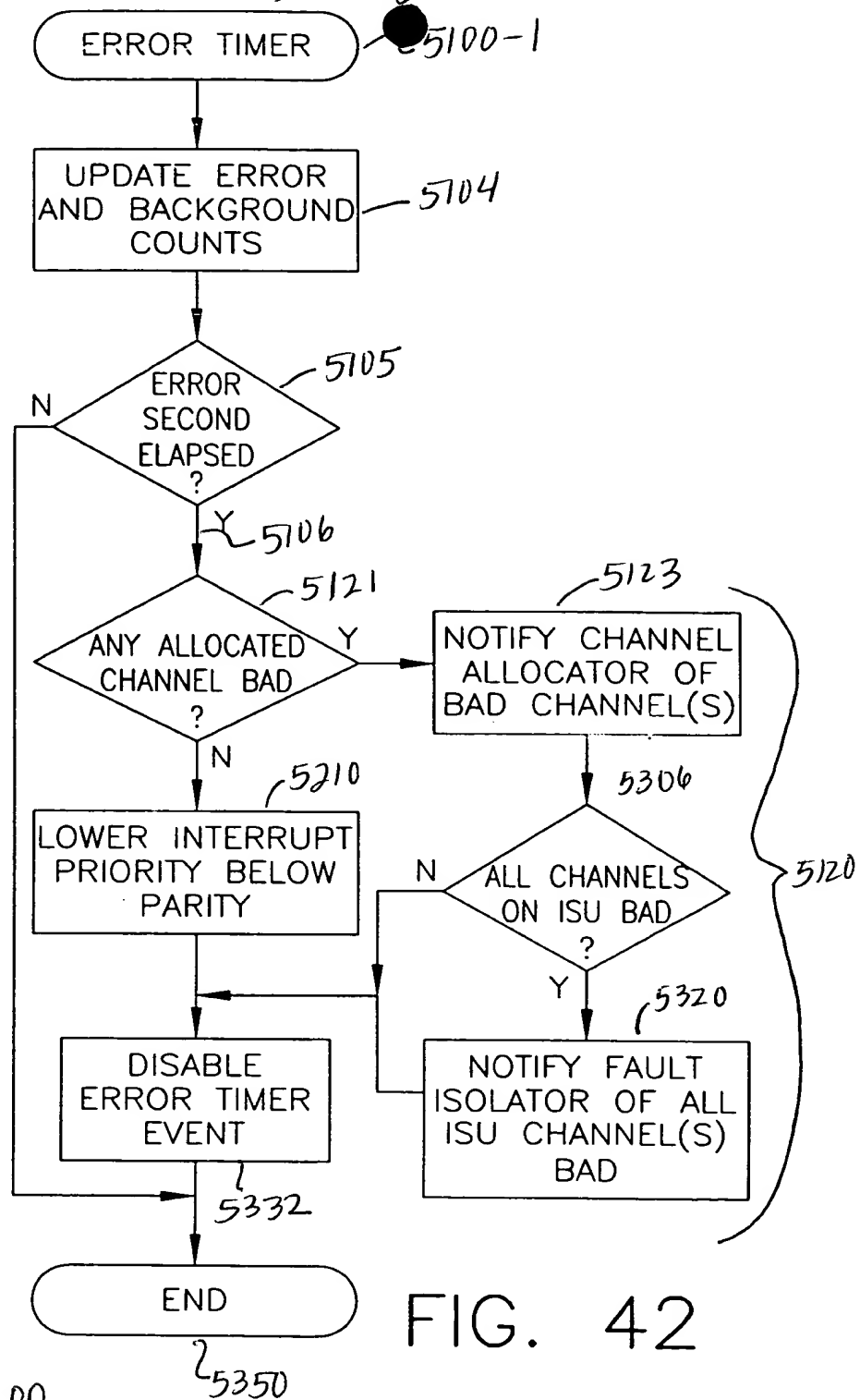
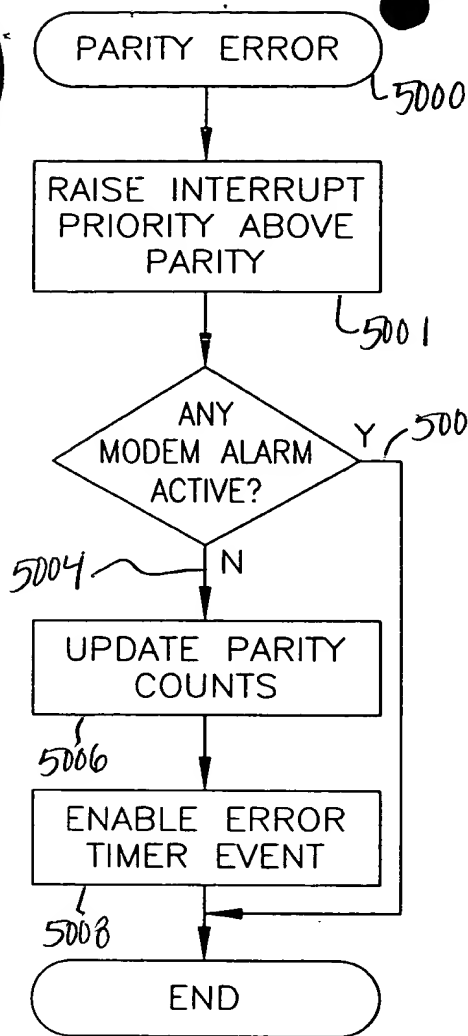
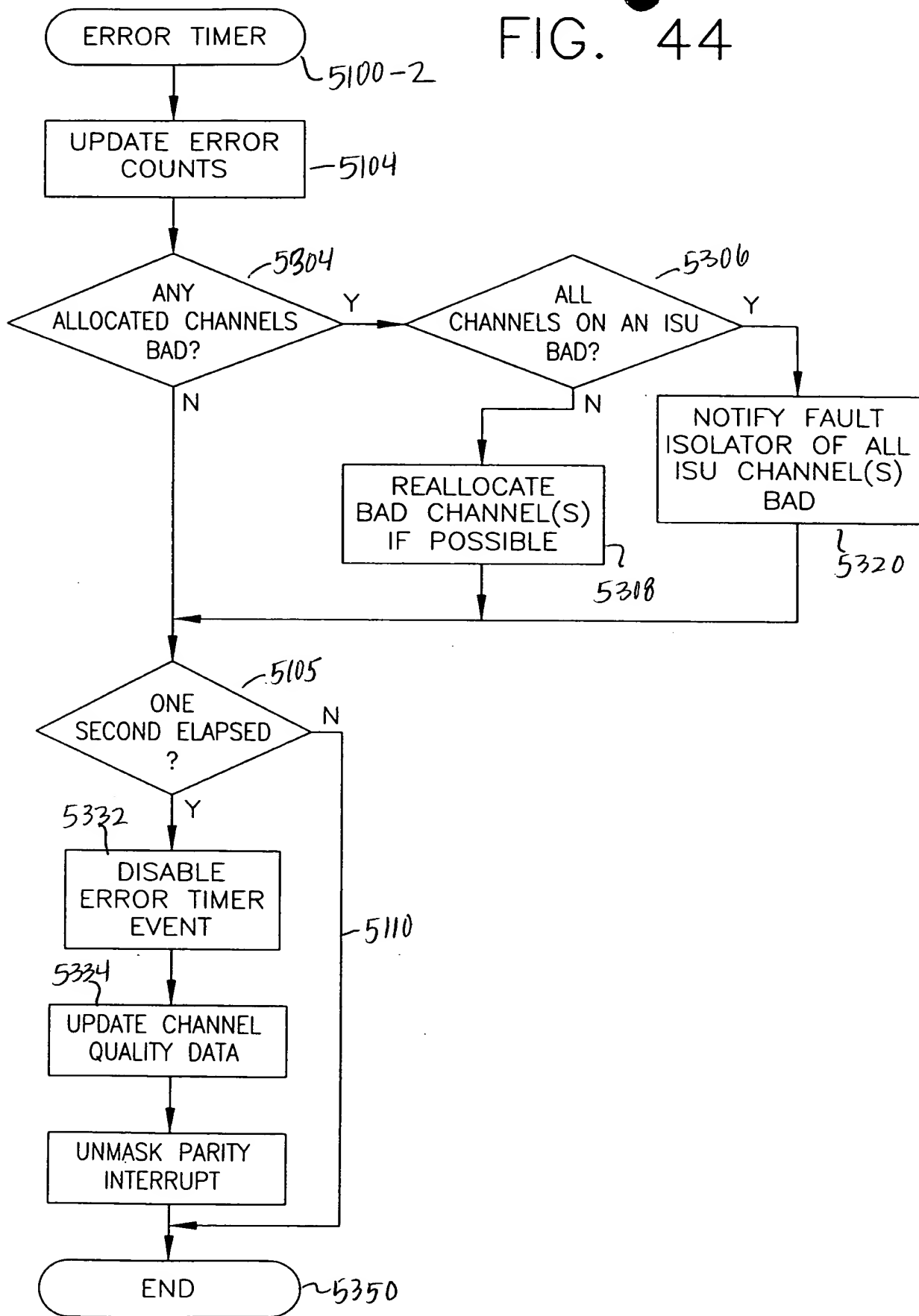




FIG. 44

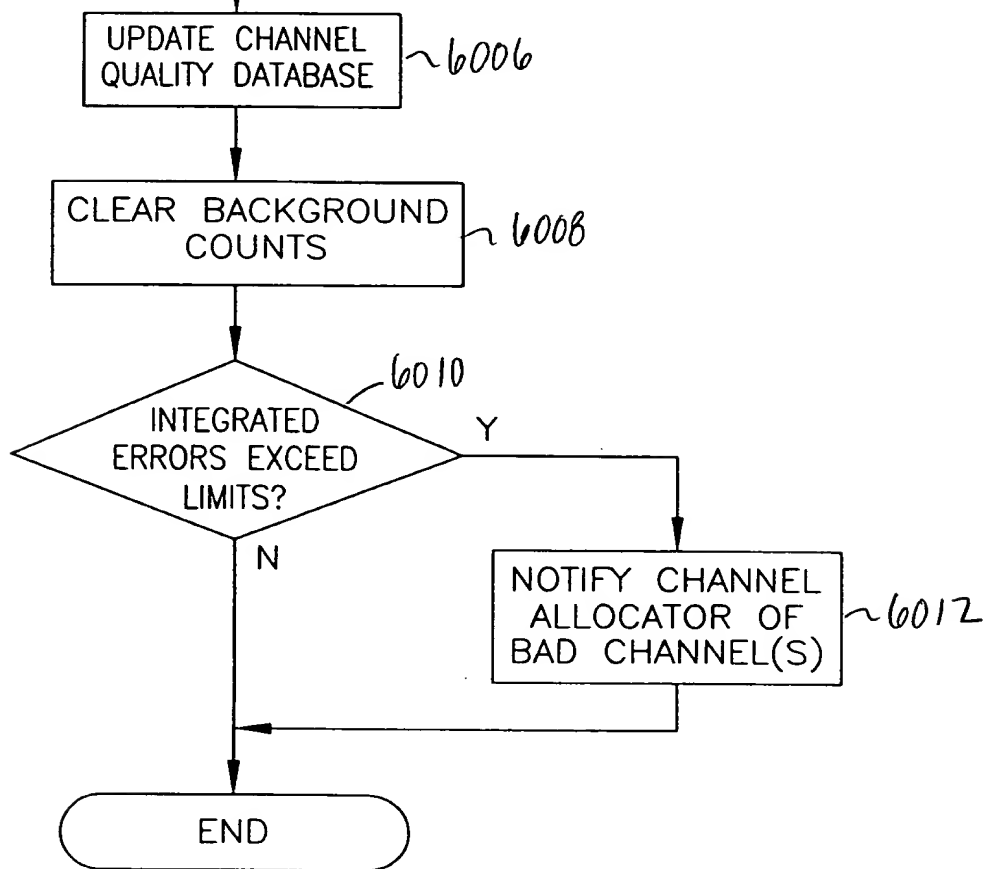




Annotated Sheet Showing Changes

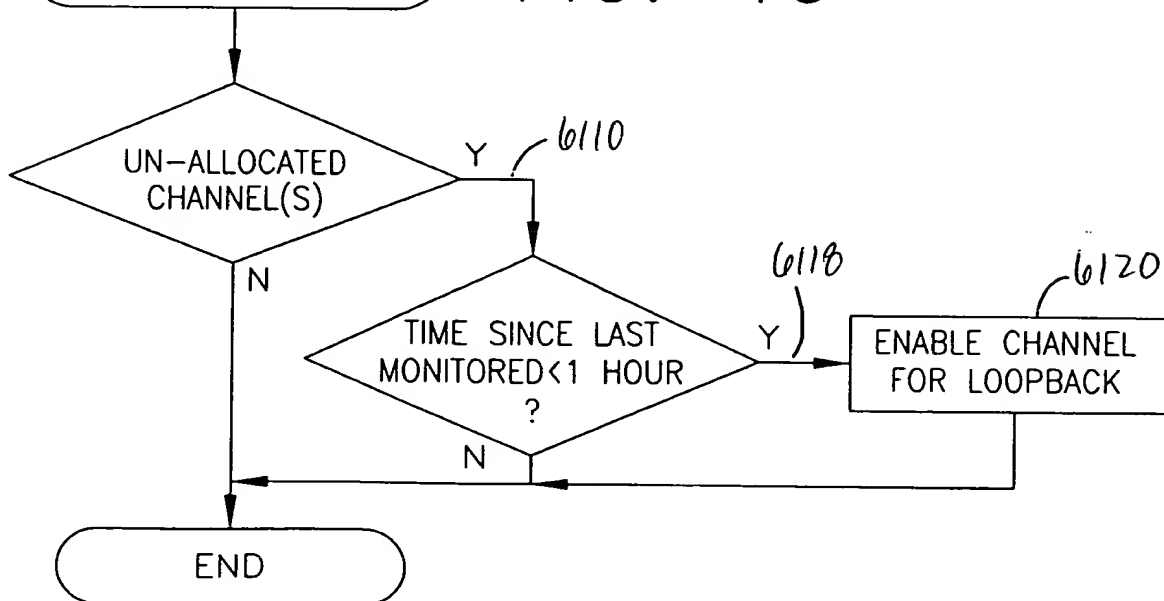
BACKGROUND TIMER

FIG. 45



BACKGROUND TIMER

FIG. 46





Annotated Sheet Showing Changes

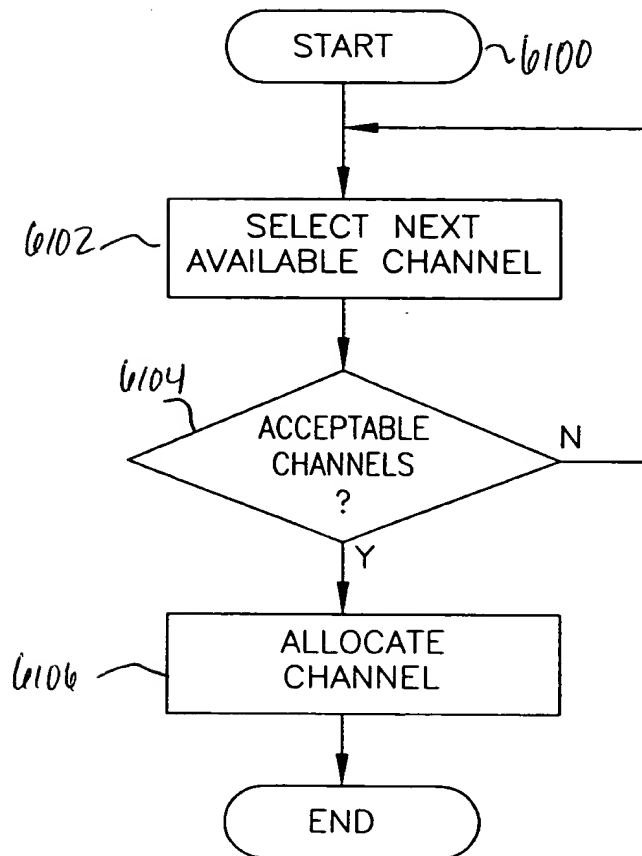


FIG. 61



Annotated Sheet Showing Changes

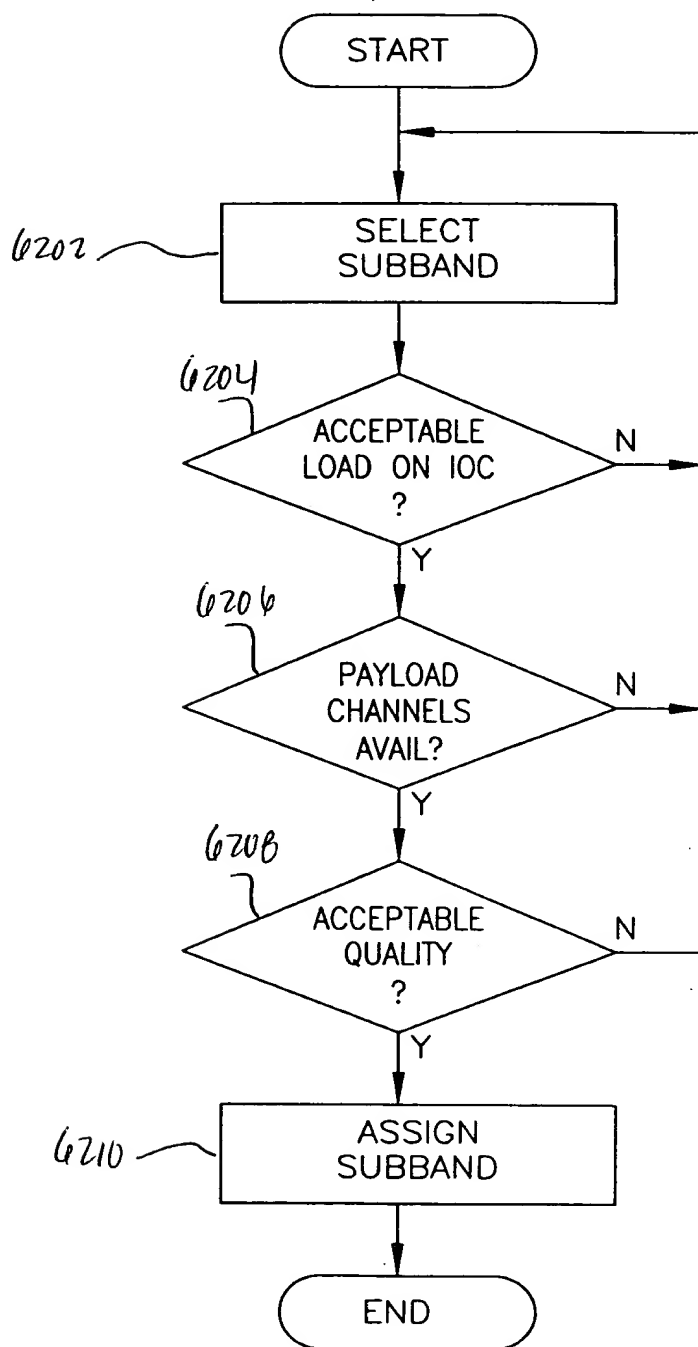


FIG. 62

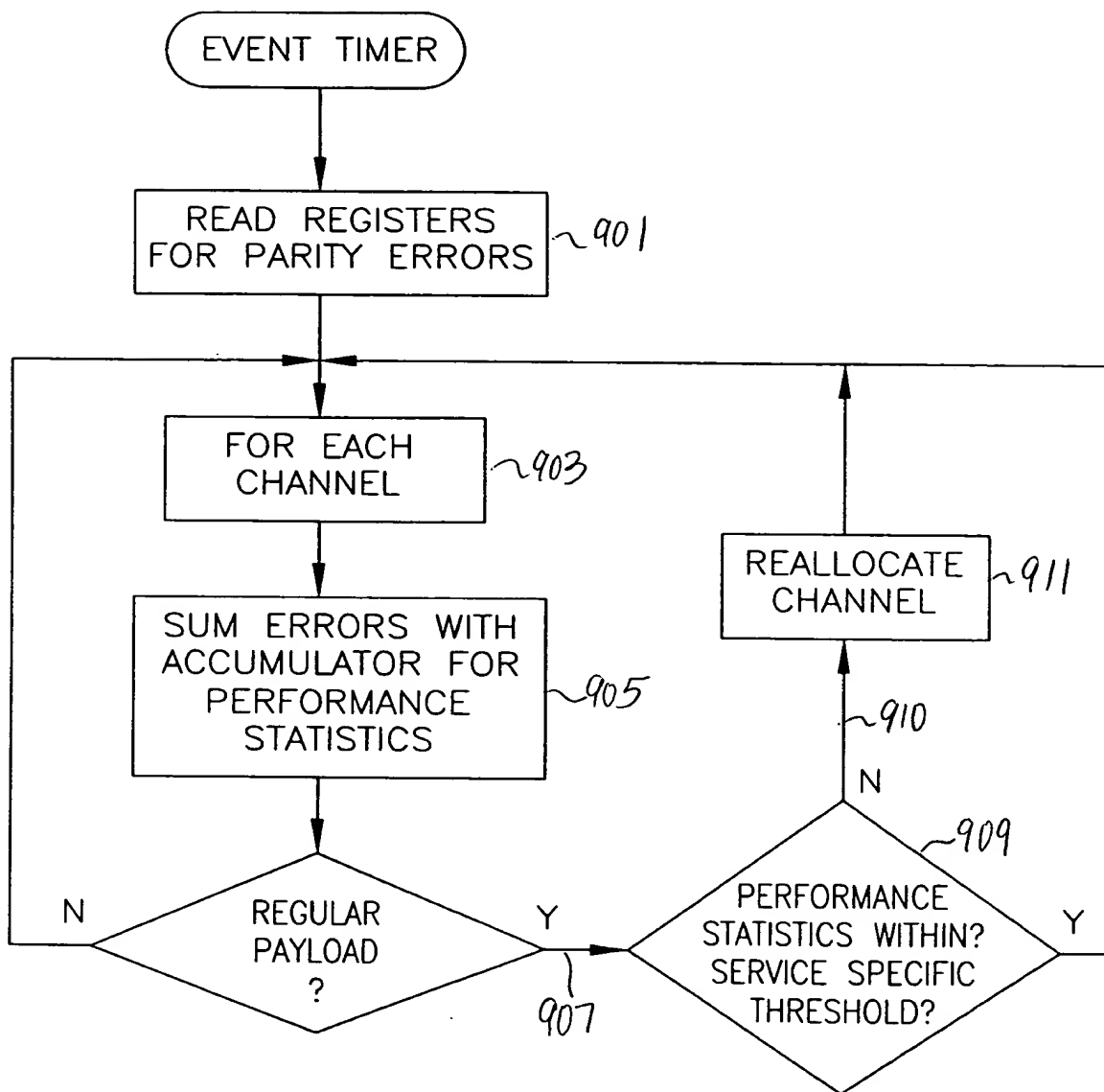


FIG. 68



● Annotated Sheet Showing Changes ●

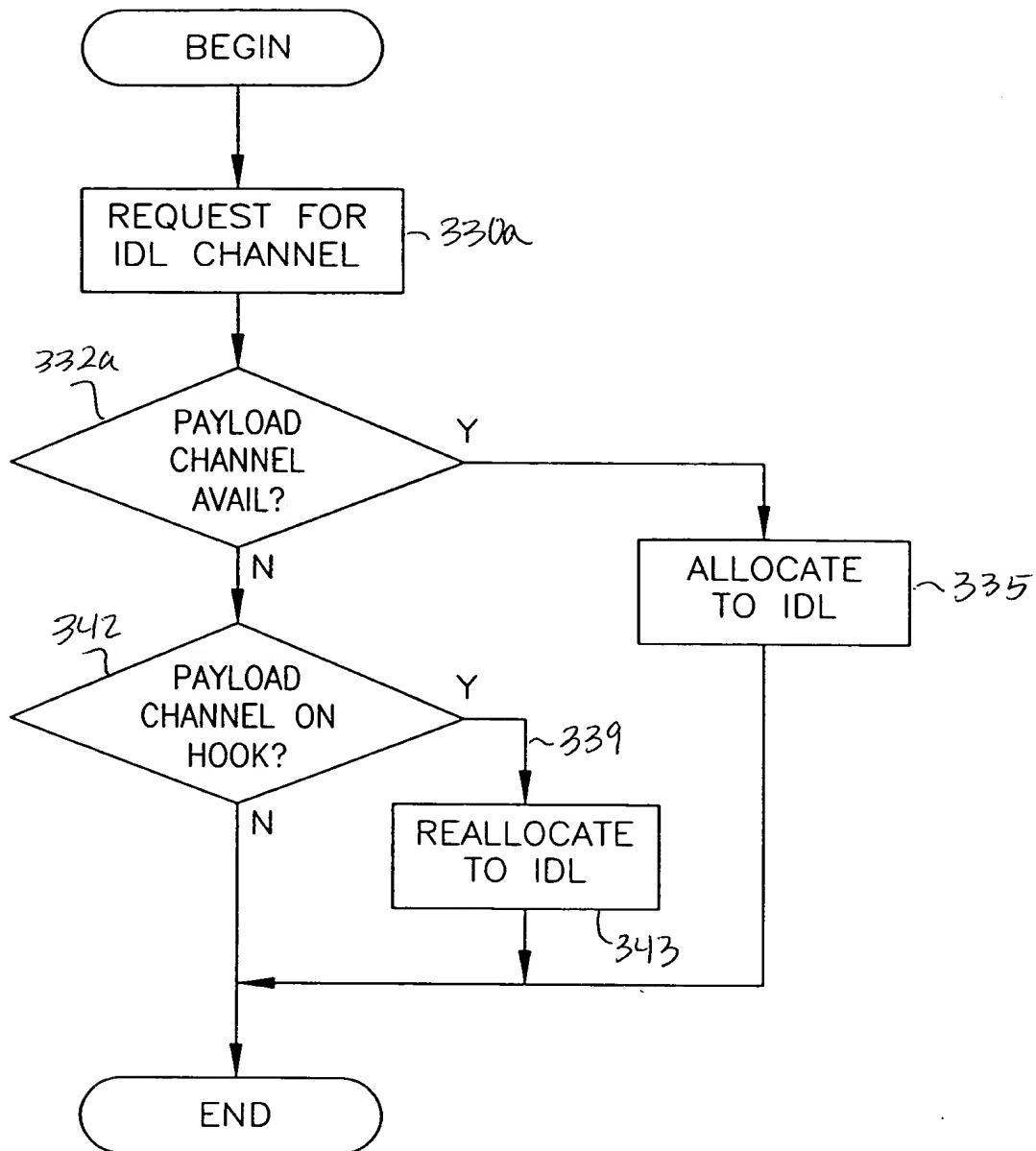


FIG. 69

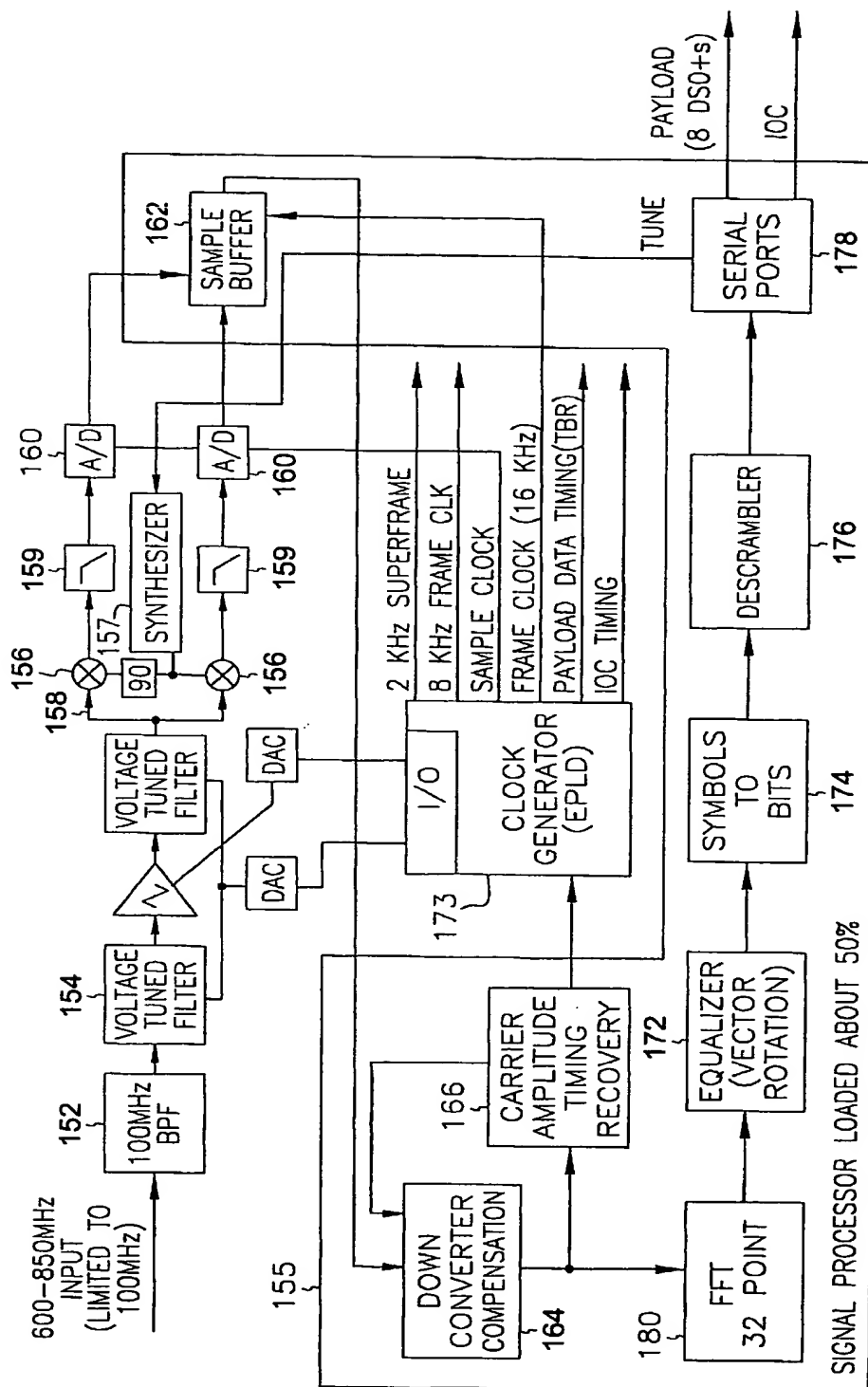


FIG. 23

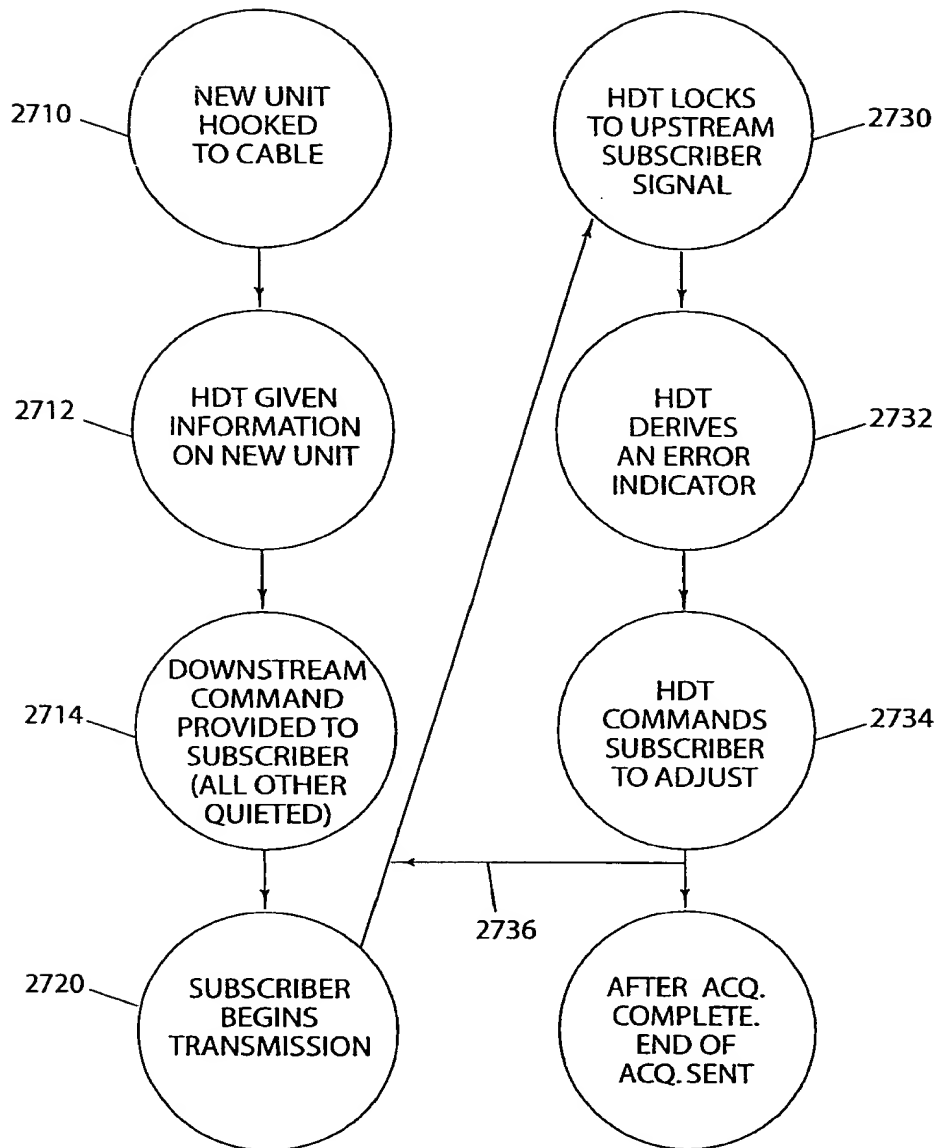


FIG. 27



Replacement Sheet

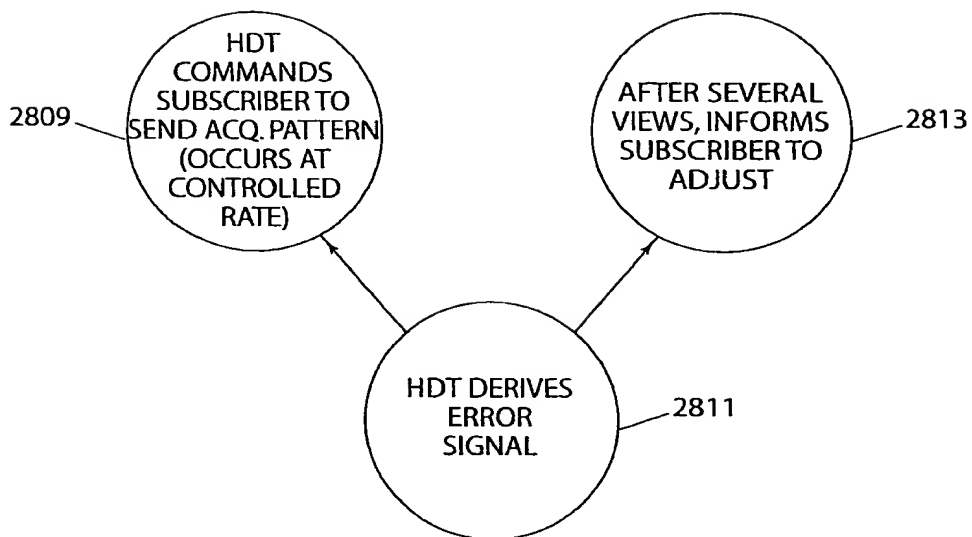


FIG. 28

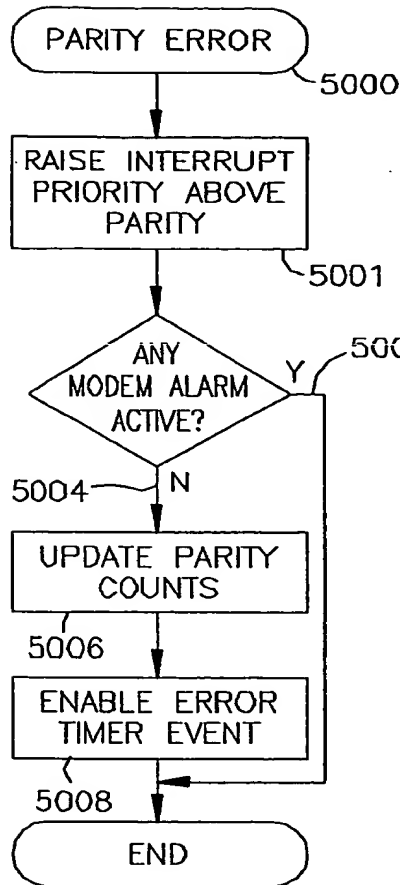


FIG. 41

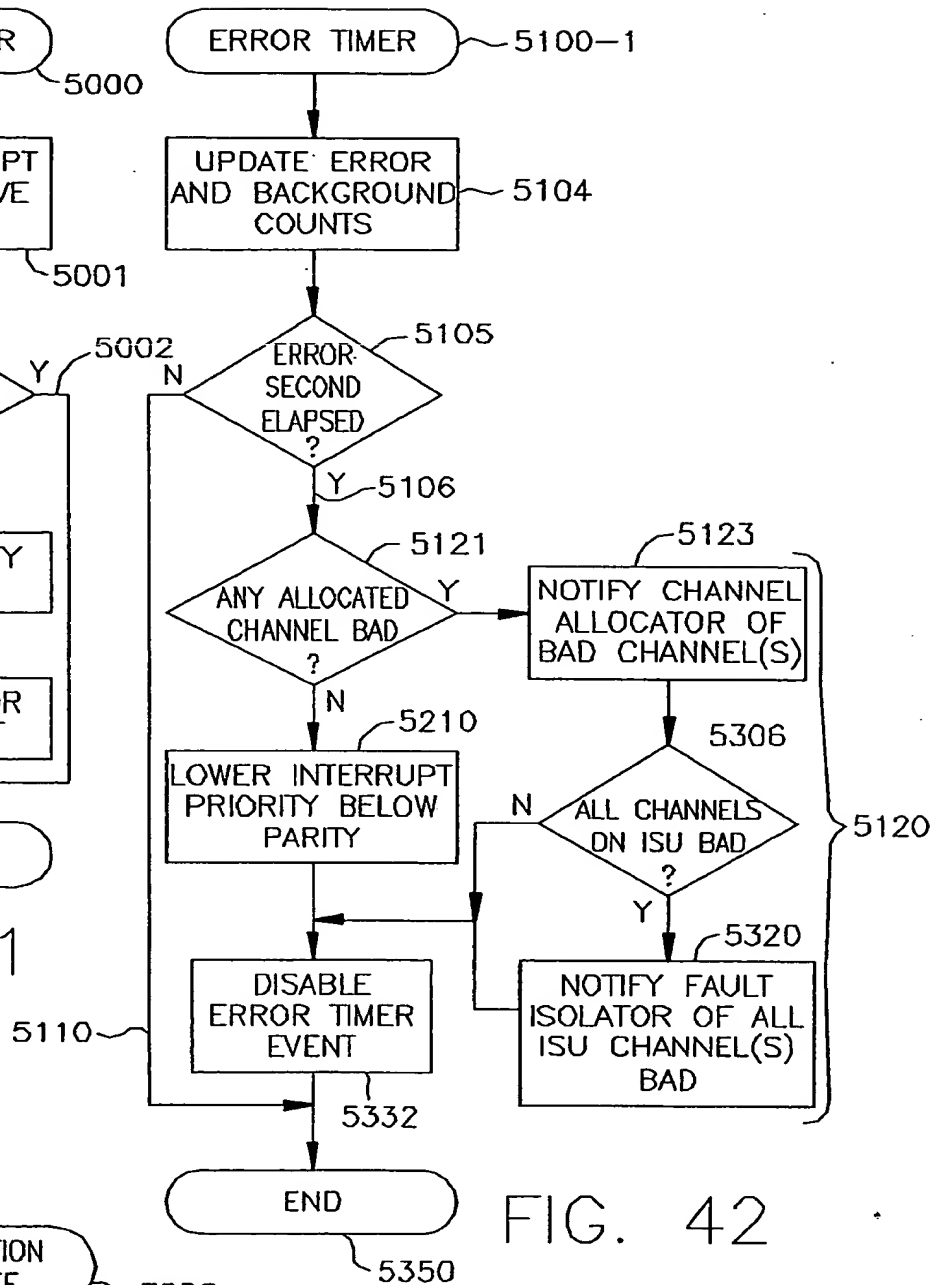


FIG. 42

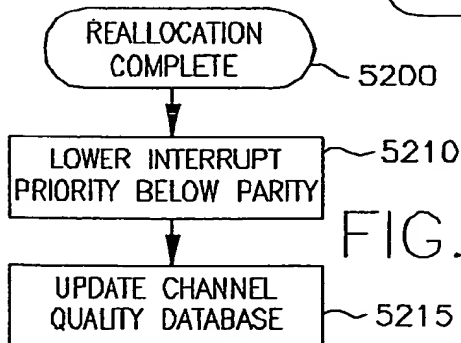


FIG. 43

FIG. 44

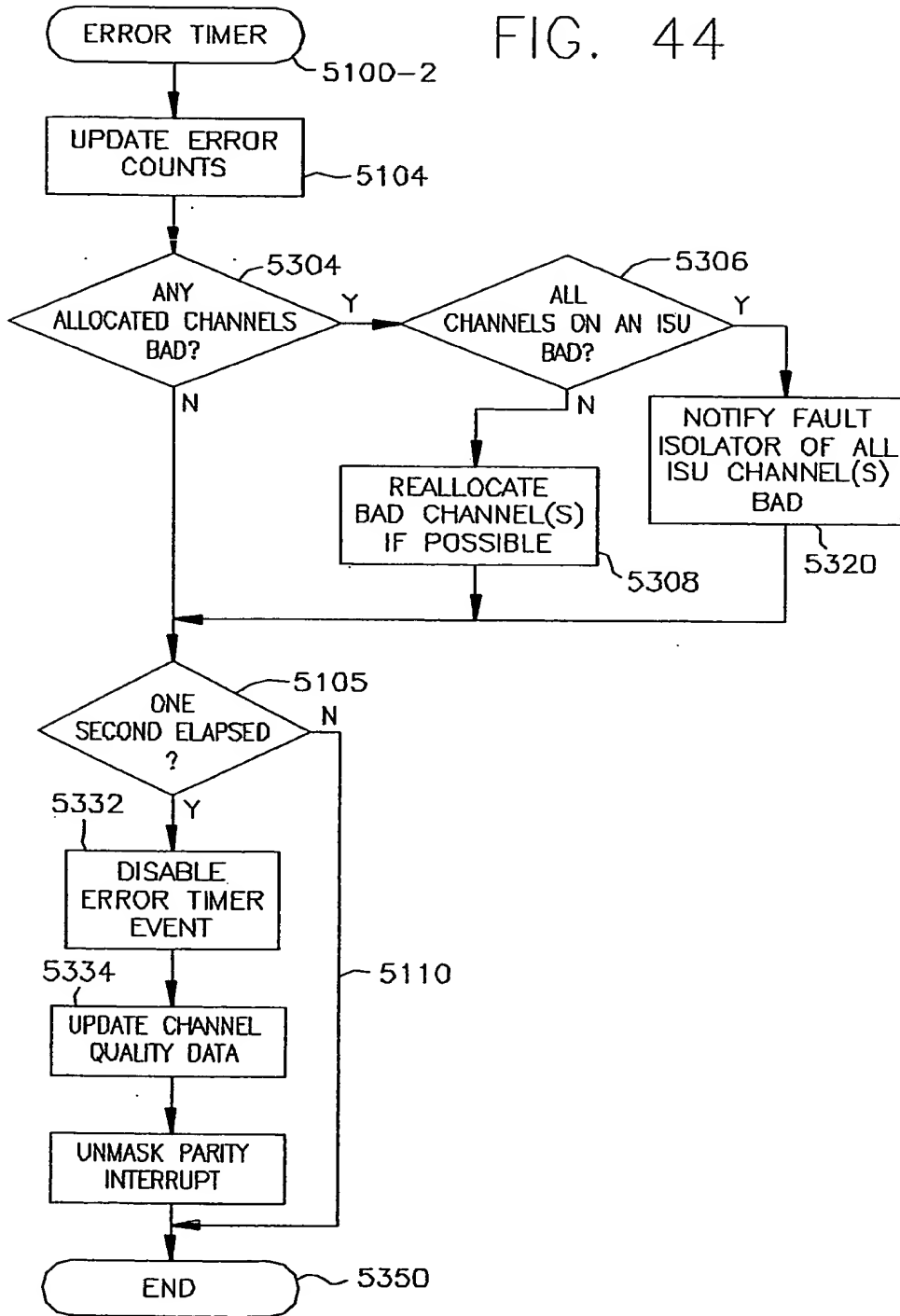


FIG. 45

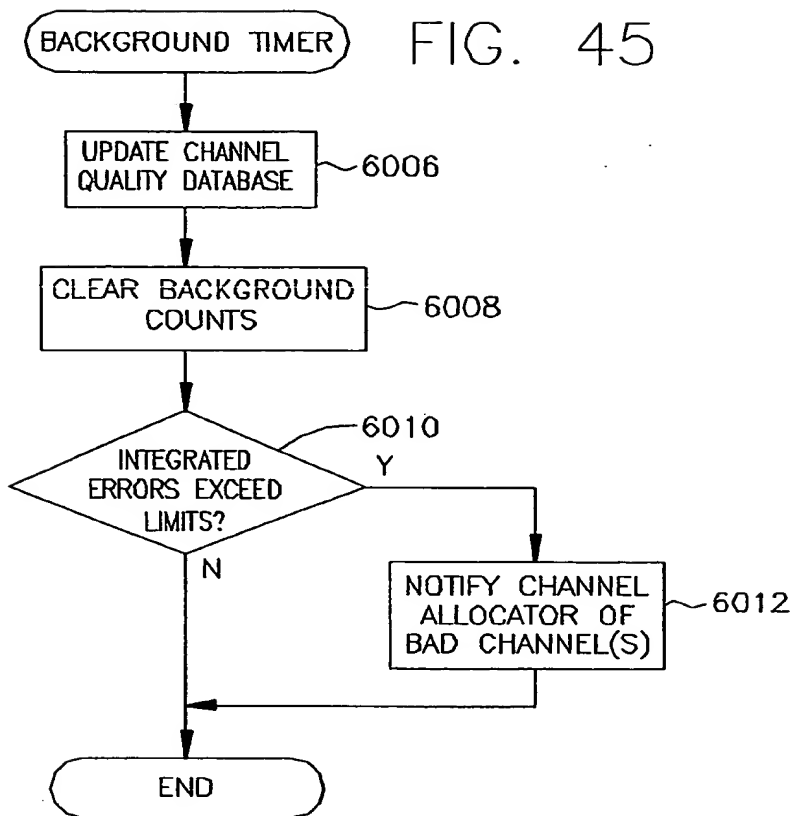
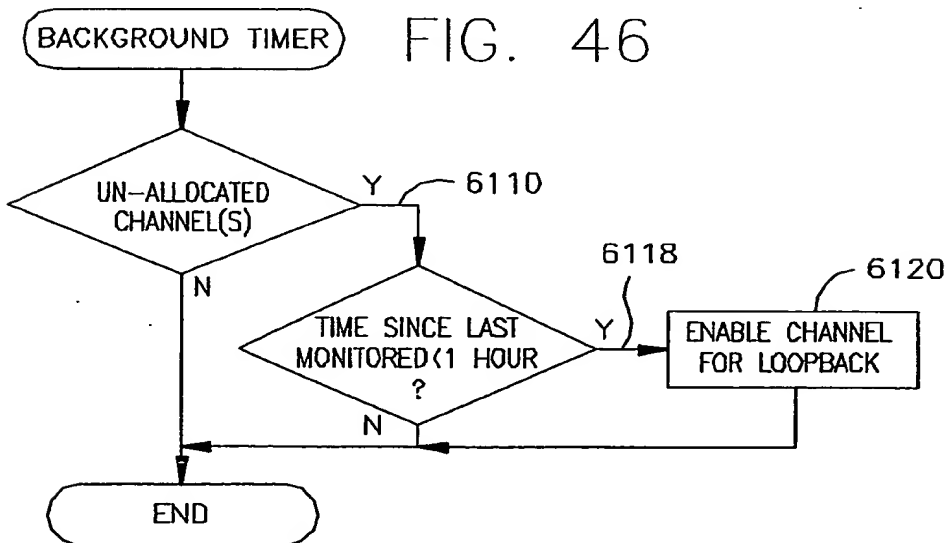


FIG. 46





Replacement Sheet

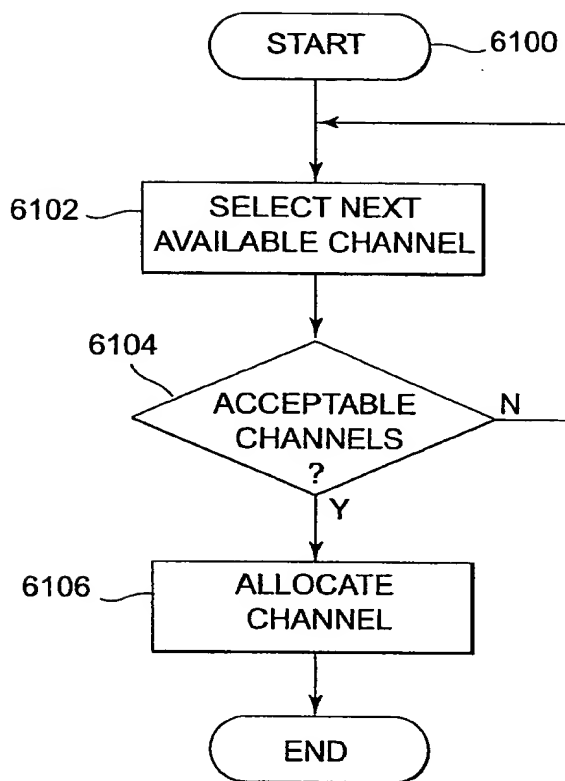


FIG. 61

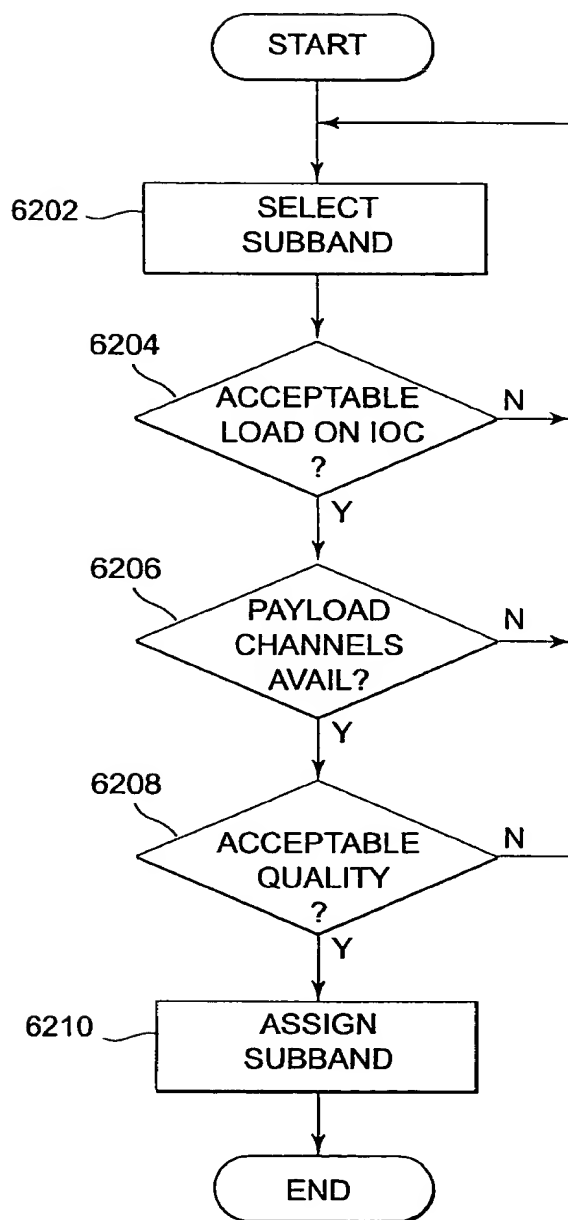


FIG. 62

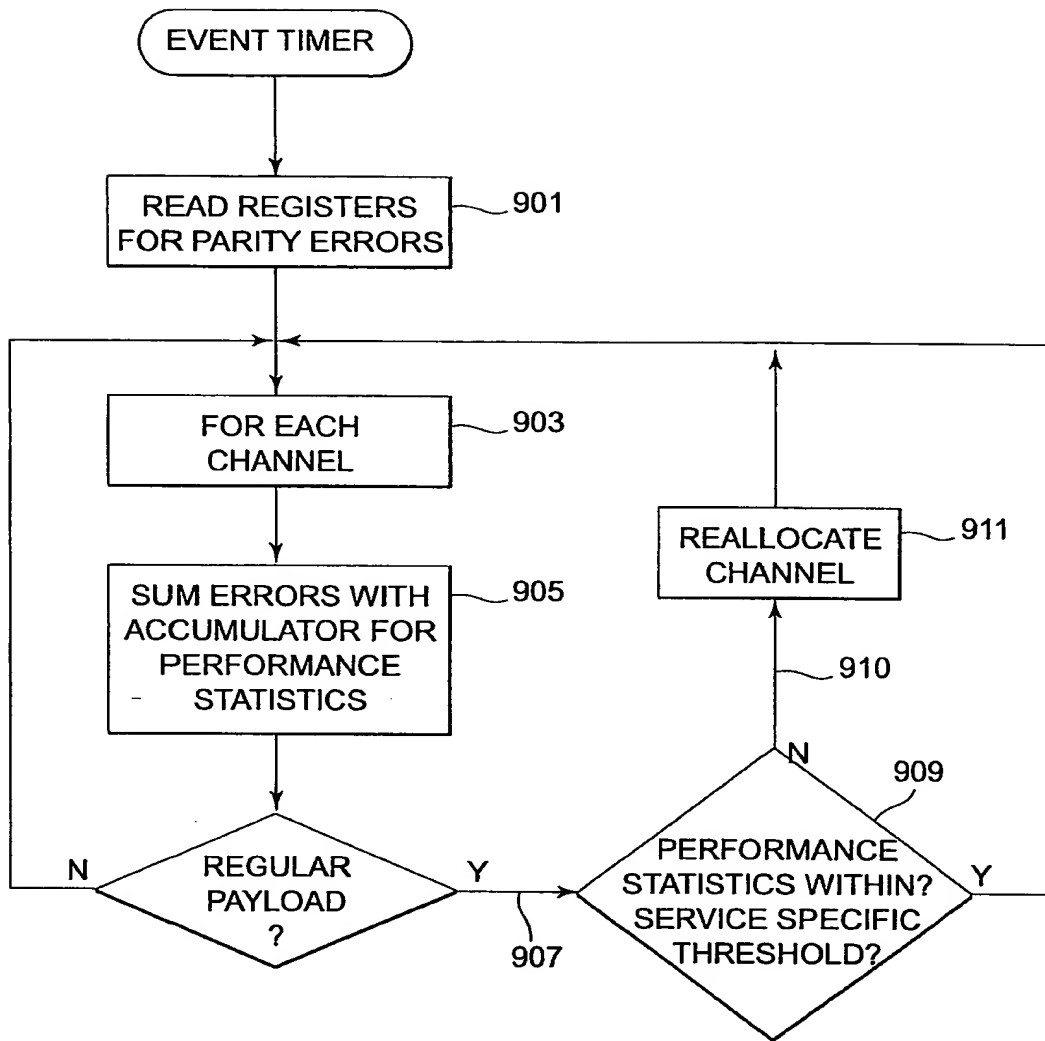


FIG. 68



Replacement Sheet

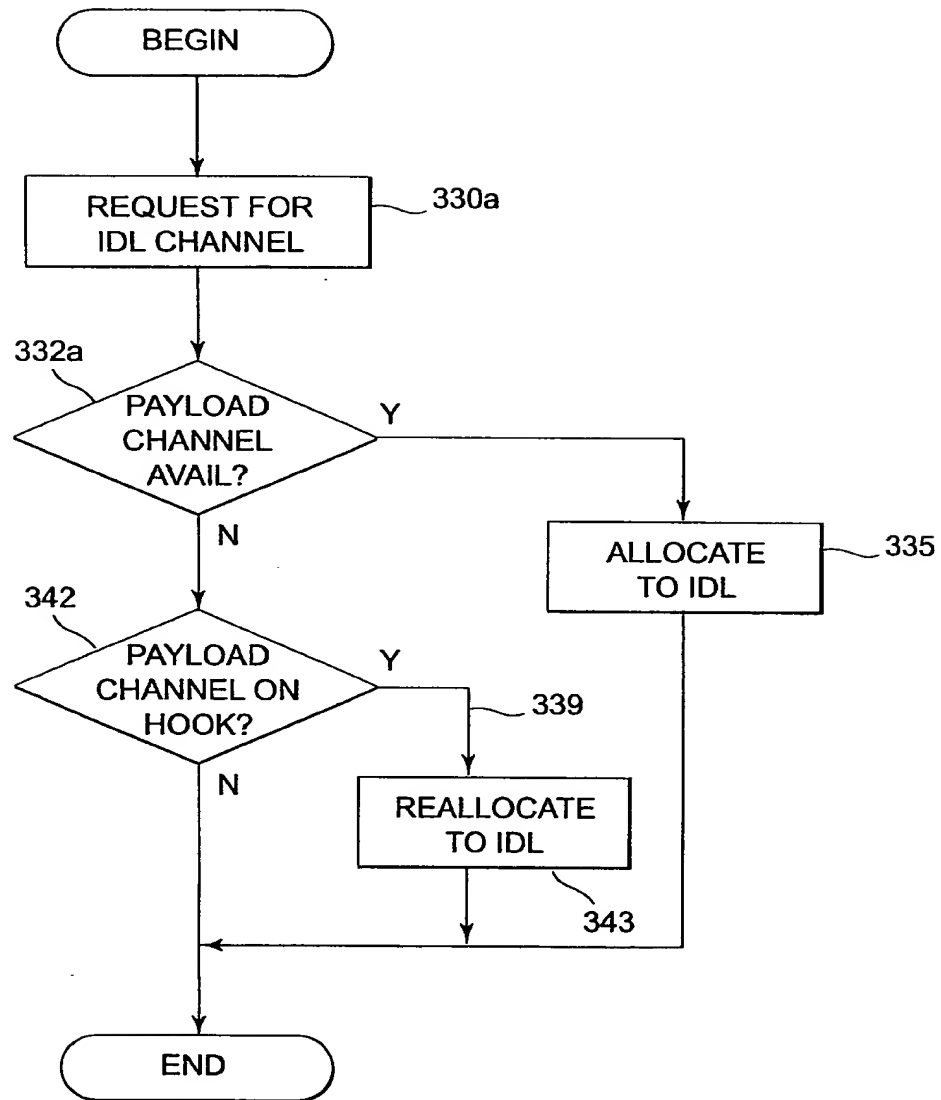


FIG. 69